Claim

What is claimed is:

1. An active matrix display device comprising:

a plurality of pixel element electrodes disposed in a matrix configuration; and

a plurality of retaining circuits disposed for the pixel element electrodes;

wherein the active matrix display device operates under two operation modes, one of said operation modes being a normal operation mode in which the pixel element electrode receives a pixel element voltage in response to an inputted image signal for presenting an analog image, another of said operation modes being a memory operation mode in which a digital image is presented based on a voltage held by the retaining circuit; and

wherein at least one of the retaining circuits is disposed as a common retaining circuit for two or more of the pixel elements, and an output of the common retaining circuit is shared by said two or more of the pixel element electrodes.

2. The active matrix display device of claim 1, wherein a common retaining circuit is disposed for every two pixel elements and the output of the common retaining circuit is shared by said every two pixel element electrodes.

3. The active matrix display device of claim 1, wherein a common retaining circuit is disposed for every four pixel elements and the output of the common retaining circuit is shared by said every four pixel element electrodes.

4. An active matrix display device comprising:

a plurality of pixel element electrodes disposed in a matrix configuration; and

a plurality of retaining circuits disposed for the pixel element electrodes;

wherein the active matrix display device operates under two operation modes, one of said operation modes being a normal operation mode in which the pixel element electrode receives a pixel element voltage in response to an inputted image signal for presenting an analog image, another of said operation modes being a memory operation mode in which a

digital image is presented based on a voltage held by the retaining circuit; and

wherein the number of the retaining circuits is smaller than the number of the pixel element electrodes.

5. The active matrix display device of claim 4, wherein the number of the retaining circuits is a half of the number of the pixel element electrodes.

6. The active matrix display device of claim 4, wherein the number of the retaining circuits is 1/4 of the number of the pixel element electrodes.

7. An active matrix display device, comprising:

An active matrix display device comprising:

a plurality of pixel element electrodes disposed in a matrix configuration; and

a plurality of retaining circuits disposed for the pixel element electrodes;

wherein the active matrix display device operates under two operation modes, one of said operation modes being a normal operation mode in which the pixel element electrode receives a pixel element voltage in response to an inputted image signal for presenting an analog image, another of said operation modes being a memory operation mode in which a digital image is presented based on a voltage held by the retaining circuit; and

wherein the number of the pixel elements for presenting the digital image under the memory operation mode is smaller than the number of the pixel elements for presenting the analog image under the normal operation mode.

8. The active matrix display device of claim 7, wherein the number of the pixel elements for display under the memory operation mode is a half of the number of the pixel element for display under the normal operation mode.

9. The active matrix display device of claim 7, wherein the number of the pixel elements for display under the memory operation mode is one fourth of the number of the

pixel element for display under the normal operation mode.

10. The active matrix display device of claim 1, 2, 3, 4, 5, 6, 7, 8 or 9, wherein the retaining circuit is a multiple-bit memory holding voltages of three or more values.